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(54) [Title of the Invention] CLOCK DRIVER CIRCUIT

(57) [Abstract]

[Object]

Preventing switching noises of clocks in different phases from being mutually affected through power supply lines.

[Construction]

A power supply line 3 and a ground line 5 that each supply a power supply to first-phase clock driver gate circuits 11 and 12 and a power supply line 4 and a ground line 6 that each supply a power supply to second-phase clock driver gate circuits 13 and 14 are wirings that are mutually independent.

[Effects]

Switching noises of clocks in different phases are prevented from being mutually affected through power supply lines, and waveforms of clocks in different phases are prevented from increasing crossover voltages thereof.

[Scope of Claim]

[Claim 1]

A clock driver circuit characterized in that, in a clock driver circuit that supplies clock signals for a plurality of phases, a power supply line and a ground line of a clock signal driving portion in each phase are mutually independent of a power supply line and a ground line of a clock signal driving portion for a different phase.

[Claim 2]

A clock driver circuit according to claim 1 characterized in that the power supply line and the ground line of the clock signal driving portion in each phase are independent in every phase.

[Claim 3]

A clock driver circuit according to claim 1 or 2 characterized in that the clock signal driving portion in the same phase is connected to a common power supply line and ground line.

[Detailed Description of the Invention]

[0001]

[Industrial Field of the Invention]

The present invention relates to a clock driver circuit, in particular, a clock driver circuit that supplies multiphase clocks to a circuit.

[0002]

[Related Art]

In a conventional clock driver circuit that is supplied with clock signals in a plurality of phases, which each differs in changing time, for example, a driver circuit of non-overlapping multiphase clocks, a clock line driving portion of each phase is supplied with a power supply by a common power supply line and ground line.

[0003]

Generally, a load capacity of a clock line is extremely large as compared with

other signal lines; therefore, a high power supply current flows in accordance with switching of the clock driver circuit. Accordingly, noises occur in a power supply line and a ground line. This power supply noise is mutually affected between non-overlapping clocks in different phases.

[0004]

For example, in a case of non-overlapping two-phase clocks when it is tried to generate a clock waveform like FIG. 3, noises like FIG. 4 occur in the waveform of a power supply line and a ground line. Consequently, clock a waveform that is outputted from a clock driver circuit is transformed like FIG. 5 and a crossover voltage in a waveform of clocks in different phases are increased.

[0005]

[Problem to be Solved by the Invention]

As described above, in the conventional non-overlapping multiphase clock circuit, switching noises of clocks in different phases are mutually affected through a power supply line and a ground line, and crossover voltages of the clock in different phases are increased. In the worst case, the crossover voltage exceeds a threshold of a switching element. Such a distortion of a clock waveform causes various malfunctions in a digital circuit.

[0006]

For example, when gate potential of a switching element is increased due to the distortion of a clock waveform, the element is in a conductive state at an unnecessary time; thus, a malfunction such as holding miss in a dynamic circuit or leak-out of a signal in a latch circuit occurs.

[0007]

The present invention is implemented in view of the above problems and, it is an object to provide a clock driver circuit where switching noises of clocks in different phases are not mutually affected through a power supply line and a ground line.

[0008]

[Means for Solving the Problem]

A clock driver circuit according to the present invention is characterized in that, in a clock driver circuit that supplies clock signals for a plurality of phases, a power

supply line and a ground line of a clock signal driving portion for each phase are mutually independent of a power supply line and a ground line of a clock signal driving portion for a different phase.

[0009]

[Operation]

In a clock driver circuit of the present invention, a power supply line and a ground line of a clock signal driving portion for each phase is not common to a power supply line and a ground line of a clock signal driving portion for a different phase; therefore, switching noises of clocks in different phases are not mutually affected through the power supply line and the ground line.

[0010]

[Embodiment]

Hereinafter, an embodiment of the present invention will be explained with reference to the accompanying drawings.

[0011]

FIG. 1 shows a configuration of a clock driver circuit that relates to one embodiment of the present invention, and a non-overlapping two-phase clock driver circuit with inverting logical output is given as an example in this embodiment.

[0012]

A clock driver circuit of FIG. 1 has a phase control circuit 2 including two NAND gates and three inverters, and clock driver gate circuits 11 to 14 each including a P-MOSFET and an N-MOSFET. The clock driver gate circuits 11 to 14 includes a first-phase positive-phase clock driver gate circuit 11, a first-phase negative-phase clock driver gate circuit 12, a second-phase positive-phase clock driver gate circuit 13, and a second-phase negative-phase clock driver gate circuit 14. The first-phase positive-phase clock driver gate circuit 11 and the first-phase negative-phase clock driver gate circuit 12 are connected to a high potential reference potential source 15 and a low potential reference potential source 16 through a common high potential power supply line, that is, a power supply line 3 and a common ground power supply line, that is, a ground line 5, respectively. The second-phase positive-phase clock driver gate circuit 13 and the second-phase negative-phase clock driver gate circuit 14 are

connected to the high potential reference potential source 15 and the low potential reference potential source 16 through a common high potential power supply line, that is, a power supply line 4 and a common ground power supply line, that is, a ground line 6, respectively. In other words, the first-phase clock driver gate circuits 11 and 12 and the second-phase clock driver gate circuits 13 and 14 which are different to each other are each supplied with a power supply from the high potential reference potential source 15 and the low potential reference potential source 16 through the power supply lines 3 and 4 and the ground lines 5 and 6 which are different to each other.

[0013]

Next, an operation of a device in this embodiment that is composed in this manner will be explained.

[0014]

An original clock that is supplied to an input terminal 1 is divided into each phase to be supplied to the clock driver gate circuits 11 to 14 after passing through the phase control circuit 2. The clock driver gate circuits 11 to 14 each drive a load through output terminals 7 to 10. The power supply lines 3 and 4 are each wired independently from the high potential reference potential source 15, and the power supply line 3 supplies high potential power supply output to the first-phase clock driver gate circuits 11 and 12 whereas the power supply line 4 supplies high potential power supply output to the second-phase clock driver gate circuits 13 and 14. The ground lines 5 and 6 are each wired independently from the low potential reference potential source 16, and the ground line 5 supplies low potential power source output, that is, ground potential to the first-phase clock driver gate circuits 11 and 12 whereas the ground line 6 supplies low potential power source output, that is, ground potential to the second-phase clock driver gate circuits 13 and 14.

[0015]

Switching is performed at the same time both in the first-phase clock driver gate circuits 11 and 12, as well as both in the second-phase clock driver gate circuits 13 and 14. In this case, since there is a gap in a switching time between the first-phase clock driver gate circuits 11 and 12 and the second-phase clock driver gate circuits 13 and 14, in a conventional case, the first-phase clock driver gate circuits and the

second-phase clock driver gate circuits are in a relation to interfere with each other due to switching noise. However, in the configuration of FIG. 1, the power supply lines 3 and 4 are independent of each other and the ground lines 5 and 6 are also independent of each other; therefore, mutual interference between each phase due to switching noises does not occur.

[0016]

Next, this situation will be explained with reference to waveforms.

[0017]

FIG. 6 is a diagram showing an example of output waveforms and power supply waveforms of a conventional clock driver circuit. A fluctuation of a power supply voltage is generated at a variation point of a first-phase clock CK1 and an inverted signal thereof CK1B. In the same manner, a fluctuation of a power supply voltage is generated at a variation point of a second-phase clock CK2 and an inverted signal thereof CK2B. Therefore, the first-phase clock and the second-phase clock are interfering with each other.

[0018]

FIG. 2 is an example of output waveforms and power supply waveforms of a clock driver circuit according to the present invention. Each of these waveforms is waveforms in the output terminals 7 and 8, the power supply line 3, the ground line 5, the power supply line 4, the ground line 6, and the output terminals 9 and 10 of FIG. 1. As shown in FIG. 6, the power supply noises that occur in the power supply line 3 and the ground line 5 at a variation point of the waveforms of the output terminals 7 and 8 in the first phase are not transmitted to the power supply line 4 and the ground line 6 in the second-phase. In the same manner, the power supply noises that occur in the power supply line 4 and the ground line 6 at a variation point of the output terminals 9 and 10 are not transmitted to the power supply line 3 and the ground line 5. Therefore, waveforms of the clock signals outputted to the output signals 7, 8, 9, and 10 are not distorted.

[0019]

Accordingly, by separating each of power supply lines and ground lines of clock signal driving portions in a plurality of phases to be independent, switching noises

that occur from the clock signal driving portion for each phase is not mutually affected through the power supply lines and the ground lines; thus, increase of a crossover voltage in waveforms of clocks in different phases can be prevented. Consequently, in a digital circuit that is controlled by clocks, a malfunction such as holding miss or leak-out of a signal, which often occurred in the conventional case, can be prevented.

[0020]

The present invention is not limited to the above embodiment and can be implemented by transforming variously like, for example, also separating a power supply line and a ground line of positive-phase and negative-phase clock driver gate circuits to be independent.

[0021]

[Effect of the Invention]

As described above, according to the present invention, by separating each of power supply lines and ground lines of clock signal driving portions for a plurality of phases to be independent, it is possible to provide a clock driver circuit where switching noises that occur from a clock signal driving portion in each phase are not mutually affected through the power supply lines and the ground lines.

[Brief Description of Drawings]

FIG. 1 is a circuit diagram showing a configuration of a clock driver gate circuit that relates to one embodiment of the present invention.

FIG. 2 is a diagram showing output waveforms and power supply waveforms of the clock driver circuit of FIG. 1.

FIG. 3 is an ideal waveform diagram of a non-overlapping two-phase clock.

FIG. 4 is a waveform diagram of a power supply including noise that occurs in a non-overlapping two-phase clock driver circuit.

FIG. 5 is an output waveform diagram of a conventional non-overlapping two-phase clock driver circuit.

FIG. 6 is a diagram showing output waveforms and power supply waveforms of a conventional clock driver circuit.

[Description of Reference]

2; phase control circuit

3, 4; high potential power supply line (power supply line)

5, 6; ground power supply line (ground line)

11 to 14; clock driver gate circuit

15; high potential reference potential source

16; low potential reference potential source